PATENT CLAIMS

1 A method for assembling a power semiconductor module, comprising the steps of:

- disposing a first electrically conductive layer (4) on at least one portion of a top surface of an electrically insulating substrate (2), so that at least one peripheral top region of said electrically insulating substrate (2) remains uncovered by the first electrically conductive layer (4);
- disposing a precursor (51) of a first electrically insulating material (5) in a first corner region (24) formed by said first electrically conductive layer (4) and said peripheral region of said electrically insulating substrate (2);
- polymerizing the precursor (51) of the first electrically insulating material (5) to form the first electrically insulating material (5);
- bonding a semiconductor chip (6) onto said first electrically conductive layer (4);
- bonding the electrically insulating substrate (2) onto a bottom plate (11);
- covering said semiconductor chip (6), said electrically insulating substrate (2), said first electrically conductive layer (4), and said first electrically insulating material (5) at least partially with a second electrically insulating material (8);

characterized in that

- the precursor (51) of the first electrically insulating material (5) is a low viscosity monomer or oligomer that forms a polyimide when polymerizing, and that
- small amounts of said precursor (51) are being applied to the junction of said first electrically conductive layer (4) and said peripheral region of said electrically insulating substrate (2).

2 The method as claimed in claim 1, characterized in that drop dispense mechanism is used for applying drops of the precursor (51) to the junction of said first electrically conductive layer (4) and said peripheral region of said electrically insulating substrate (2), and that the precursor distributes itself along said junction by capillary forces.

3 The method as claimed in claim 1, characterized in that the electrically insulating substrate (2) is bonded onto a bottom plate (11) before the second electrically insulating material (8) is applied.

4 The method as claimed in one of the previous claims, further comprising the steps of

- disposing at least one second electrically conductive layer (3) between the bottom plate (11) and at least one portion of a bottom surface of the electrically insulating substrate (2), so as to selectively expose at least one peripheral bottom region of the electrically insulating substrate (2); and
- disposing a precursor of a third electrically insulating material in a second corner (23) formed by the second electrically conductive layer (3) and the peripheral bottom region of the electrically insulating substrate (2).

5 The method as claimed in one of the previous claims, characterized in that the precursor of the third electrically insulating material is identical to the precursor of the first electrically insulating material.

6 The method as claimed in one of the previous claims, characterized in that a primer is disposed to at least partially cover the semiconductor chip (6), the electrically insulating substrate (2), the first electrically conductive layer (4), and the first electrically insulating material (5) before the second insulating material is attached.

7 A power semiconductor module, comprising:

- an electrically insulating substrate (2)
- a first electrically conductive layer (4) disposed on at least one portion of a top surface of said electrically insulating substrate (2), so as to selectively expose at least one peripheral top region of said electrically insulating substrate (2);
- at least one semiconductor power chip mounted on said electrically conductive layer (4);
- a first electrically insulating material (5) disposed in a corner region formed by said first electrically conductive layer (4) and said peripheral region of said electrically insulating substrate (2);

- a second insulating material (8) at least partially embedding said semiconductor power chip, said electrically insulating substrate (2), said first electrically conductive layer (4), and said first electrically insulating material (5);

characterized in that

- the first electrically insulating material (5) is a polyimide, and
- the surface of the first electrically insulating material (5) disposed in the corner region formed by said first electrically conductive layer (4) and said peripheral region of said electrically insulating substrate (2) is concave-shaped.

8 The power semiconductor module as claimed in claim 7, characterized in that the electrically insulating substrate (2) is mounted on a bottom plate (11).

9 The power semiconductor module as claimed in claim 7 or 8, characterized in that at least one second electrically conductive layer (3) is disposed between the bottom plate (11) and at least one portion of a bottom surface of the electrically insulating substrate (2), so as to selectively expose at least one peripheral bottom region of the electrically insulating substrate (2); and that a third insulating material (9) is disposed in a second corner (23) formed by the second electrically conductive layer (3) and the peripheral bottom region of the electrically insulating substrate (2).

10 The power semiconductor module as claimed in claim 7, 8 or 9, characterized in that a rigid layer (7) of resin is provided between the second electrically insulating material (8) and the semiconductor chip (6), the substrate (2), the first conductive layer (4) and the first electrically insulating material (5).